Claims

What is claimed:

1. A full duplex transceiver for transmitting and receiving communication signals, the transceiver comprising:

1 to N sample and hold circuits, each sample and hold circuit receiving a first signal comprising a far-end signal; and

a plurality of subtraction circuits, each subtraction circuit receiving an output of at least one of the sample and hold circuits, each subtraction circuit subtracting at least a fraction of a replica signal from at least a fraction of the output of the at least one of the sample and hold circuits.

2. The full duplex transceiver of claim 1, wherein each sample and hold circuit additionally receives a replica signal, and each subtraction circuit receives a sample and hold replica signal from an output of a corresponding sample and hold circuit.

3. The full duplex transceiver of claim 1, wherein each subtraction circuit receives at least one of N replica signals, the replica signals having a replica signal frequency that is lower than a signal frequency of the first signal.

4. The full duplex transceiver of claim 1, wherein the output of the at least one sample and hold circuits is subjected to analog processing before being received by the subtraction circuit.

5. The full duplex transceiver of claim 1, wherein the replica signal is subjected to analog processing before being received by the subtraction circuit.

6. The full duplex transceiver of claim 1, wherein the first signal comprises the far-end signal, and an echo signal.

7. The full duplex transceiver of claim 1, wherein the first signal comprises the far-end signal, and cross-talk signals.

8. The full duplex transceiver of claim 1, wherein the ith sample and hold circuit receives an ith clock signal.

9. The full duplex transceiver of claim 1, wherein each subtraction circuit generates an analog output, a combination of the analog outputs of the subtraction circuits generating a representation of the far end signal.

10. The full duplex transceiver of claim 1, wherein the ith subtraction circuit receives the ith clock signal.

11. The full duplex transceiver of claim 1, wherein the subtraction circuits are continuous time circuits.

12. The full duplex transceiver of claim 1, wherein output signals of the subtraction circuits are received by analog to digital converters (ADC)s, the ADCs generating a digital output representing the far end signal.

13. The full duplex transceiver of claim 1, wherein an ith ADC receives the ith clock signal.

14. The full duplex transceiver of claim 1, further comprising a clock generation circuitry, the clock generation circuitry generating N clock signals, wherein a phase of the clock signals are spaced apart from each other by approximately (360/N) degrees.

15. The full duplex transceiver of claim 1, wherein the first signal further includes cross-talk signals.

16. A method of receiving a first signal with a full duplex transceiver, the first signal comprising a far end signal, the method comprising:

sampling and holding N versions of the first signal;

generating N replica signals;

subtracting at least a fraction of each of the N replica signals from at least a fraction of the N sample and hold versions of the first signal generating N versions of the far end signal.

17. The method of receiving a far end signal of claim 16, wherein the first signal comprises the far-end signal and an echo signal.

18. The method of receiving a far end signal of claim 16, wherein the first signal comprises the far-end signal and cross-talk signals.

19. The method of receiving a far end signal of claim 16, wherein the first signal comprises the far-end signal, an echo signal and cross-talk signals.

20. The method of receiving a far end signal of claim 16, further comprising combining the versions of the far end signal.

21. The method of receiving a far end signal of claim 16, wherein the sampling and holding is driven by a clock frequency of Fs/N, where Fs is a frequency greater than twice the frequency of the highest frequency component of the far end signal.

22. The method of receiving a far end signal of claim 16, further comprising:

programmably controlling an amplitude of the far end signals.

23. The method of receiving a far end signal of claim 16, further comprising:

generating digital samples of analog versions of the far end signal.

24. The method of receiving a far end signal of claim 16, wherein the ith sample and hold circuit receives an ith clock signal.

25. The method of receiving a far end signal of claim 16, wherein each subtraction circuit generates an analog output, a combination of the analog outputs of the subtraction circuits generating a representation of the far end signal.

26. The method of receiving a far end signal of claim 16, wherein the ith subtraction circuit receives an ith clock signal.

27. The method of receiving a far end signal of claim 16, wherein the subtraction circuits are continuous time circuits.

28. The method of receiving a far end signal of claim 16, wherein output signals of the subtraction circuits are received by analog to digital converters (ADC)s, the ADCs generating a digital output representing the far end signal.

29. The method of receiving a far end signal of claim16, wherein an ith ADC receives an ith clock signal.

30. The method of receiving a far end signal of claim 16, further comprising generating N clock signals, wherein a phase of the clock signals are spaced apart from each other by approximately (360/N) degrees.

31. A network line card, the network line card comprising a full duplex transceiver, the full duplex transceiver comprising:

1 to N sample and hold circuits, each sample and hold circuit receiving a first signal comprising a far-end signal; and

a plurality of subtraction circuits, each subtraction circuit receiving an output of at least one of the sample and hold circuits, each subtraction circuit subtracting at least a fraction of a replica signal from at least a fraction of the output of the at least one of the sample and hold circuits.

32. A server comprising a full duplex transceiver, the full duplex transceiver comprising:

1 to N sample and hold circuits, each sample and hold circuit receiving a first signal comprising a far-end signal; and

a plurality of subtraction circuits, each subtraction circuit receiving an output of at least one of the sample and hold circuits, each subtraction circuit subtracting at least a fraction of a replica signal from at least a fraction of the output of the at least one of the sample and hold circuits.

33. A LAN system comprising full duplex transceiver, the full duplex transceiver comprising:

1 to N sample and hold circuits, each sample and hold circuit receiving a first signal comprising a far-end signal; and

a plurality of subtraction circuits, each subtraction circuit receiving an output of at least one of the sample and hold circuits, each subtraction circuit subtracting at least a fraction of a replica signal from at least a fraction of the output of the at least one of the sample and hold circuits.